What is claimed is:

1. In an addressable random access memory having a plurality of data array banks arranged in columns and rows, having provision for read and write signals to said banks in separate command cycles multiplexed into a common data bus under control of the control and decoding circuitry of said columns and having power driver elements for each of said banks, the improvement for calibration of the impedance of said driver elements comprising:

means for providing, during a write command cycle, an adjust signal operable to disable input from said common data bus into said array bank, and to disconnect said write command signal from the circuitry of said columns,

means for delivering impedance control vector signals, indicating at least one of change of magnitude and of satisfaction with the present impedance state, to each of said power driver elements, and,

means for producing impedance control instructions on said common data bus, said instructions being operable to select from tabulated values of said at least one of change of magnitude and of satisfaction with the present impedance state, and delivering said instructions to said impedance control vector delivery means.

2. The addressable random access memory improvement of claim 1 wherein said data array banks are of the dynamic random access type known in the art as DRAMs.

3. An addressable random access memory array of the type having

a plurality of data banks arranged in columns and rows,

provision for read and write signals to said banks being in separate command cycles,

said read and write signals being multiplexed into a common data bus under control of the control and decoding circuitry of said columns, and,

said array having power driver elements for each of said banks,

the improvement for calibration of the impedance of said driver elements comprising:

means for providing, during a write command cycle, an adjust signal,

said adjust signal being operable

to disable input from said common data bus into said array bank, and,

to disconnect said write command signal from the circuitry of said columns,

means for delivering impedance control vector signals to each of said power driver elements

said impedance control vector signals indicating at least one of change of magnitude and of satisfaction with the present impedance state, and,

means for producing impedance control instructions on said common data bus,

said impedance control instructions operable

for selection from tabulated values of said at least one of

change of magnitude and of satisfaction with the present impedance state, and

delivering said instructions to said impedance control vector delivery means.

4. The addressable random access memory improvement of claim 3 wherein said data array banks are of the dynamic random access type known in the art as DRAMs.

5. The method of calibrating the impedance of power driving elements that drive read and write operations in an addressable random access memory array having a plurality of data banks arranged in columns and rows, having provision for read and write signals to said data banks in separate command cycles multiplexed onto a common data bus under control of the control and decoding circuitry of said columns and having power driving elements for each of said data banks,

comprising the steps of:

providing, during a write command cycle, an adjust signal, operable to disable input from said common data bus into said data banks, and to disconnect said write command signal from the circuitry of said columns,

producing impedance control instructions, said instructions being operable to select from tabulated values of said at least one of change of magnitude and of satisfaction with the present impedance state, and,

delivering said instructions to said each of said power driving elements.

6. The method of calibrating the impedance of power driving elements of claim 5 wherein: in said step of producing impedance control instructions, the added step of delivering said impedance control instructions in the form of vector signals, indicating at least one of change of magnitude and of satisfaction with the present impedance state, to each of said power driving elements.

7. The method of calibrating the output impedance of separate power drivers that drive the read and write operations in an addressable random access memory array, said memory array being of the type wherein:
there is a plurality of data banks arranged in columns and rows:
there are read and write signals to said data banks in separate command cycles multiplexed onto a common data bus under control of the control and decoding circuitry of said columns:
and there is a separate power driving element for each bank of said data banks,
comprising the steps of:
providing, during a write command cycle, an adjust signal,
said adjust signal being operable
to disable input from said common data bus into said data banks, and,
to disconnect said write command signal from the circuitry of said columns,
producing impedance control instructions,
said impedance control instructions being operable
to select from tabulated values of at least one
of change of impedance magnitude, and,
of satisfaction with the present impedance state, and,
delivering said impedance control instructions to
each of said separate power driving elements.

8. The method of calibrating the impedance of power driving elements of claim 7 wherein: in said step of producing impedance control instructions, the added step of delivering said impedance control instructions in the form of vector signals, indicating at least one of change of magnitude and of satisfaction with the present impedance state, to each of said power driving elements.

9. In an addressable random access memory array having a plurality of data banks arranged in columns and rows, wherein there is provision for read and write signals to said banks in separate command cycles multiplexed onto a common data bus and there are separate power driver elements for each of said banks,
the improvement for calibration of the impedance of each driver element of said driver elements comprising:
means for providing, during a write command cycle, adjust up and adjust down signals operable to provide clocked latched and decoded input to each said driver element as impedance control vector signals, indicating at least one of change of magnitude and of satisfaction with the present impedance state, to each of said power driving elements.

10. The addressable random access memory improvement of claim 9 wherein said data array banks are of the dynamic random access type known in the art as DRAMs.

11. In an addressable random access memory array,
said array including
a plurality of data banks arranged in columns and rows,

provision for delivery of read and write signals to said banks in separate command cycles multiplexed onto a common data bus, and, a separate power driving element for each of said data banks, the improvement for calibration of the impedance of said driver elements comprising:

means for providing an adjust up and an adjust down calibrating adjustment signal to each of said driver elements, during said command cycle for said write signal, said adjust up and an adjust down calibrating adjustment signal being operable at each said driver element as an impedance control vector signal, indicating at least one of change of magnitude and of satisfaction with the present impedance state.

12. The addressable random access memory improvement of claim 11 wherein said data array banks are of the dynamic random access type known in the art as DRAMs.